ABSTRACT OF THE DISCLOLSURE

A scanning circuit having such a high operation margin for the phase deviation of clock signal that its operation is stable. The scanning circuit includes a bidirectional shift register having transfer gates of a transfer unit and a feedback circuit, the operation of which is controlled by four phase clocks. The scanning circuit comprises a delay circuit (101) that delays control clocks (A, B) supplied to the transfer gates of the transfer unit (103) relative to control clocks (C, D) supplied to the feedback circuit (104).